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TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

524,288-WORD BY 8-BIT STATIC RAM

DESCRIPTION

The TC55NEM208AFPV/AFTV is a 4,194,304-bit static random access memory (SRAM) organized as 524,288 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.7 to 5.5 V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz (typ) and a minimum cycle time of 55 ns. It is automatically placed in low-power mode at 1 μ A standby current (typ) when chip enable (\overline{CE}) is asserted high. There are two control inputs. \overline{CE} is used to select the device and for data retention control, and output enable (\overline{OE}) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range of -40° to 85°C, the TC55NEM208AFPV/AFTV can be used in environments exhibiting extreme temperature conditions. The TC55NEM208AFPV/AFTV is available in a standard plastic 32-pin small-outline package (SOP) and normal and reverse pinout plastic 32-pin thin-small-outline package (TSOP).

FEATURES

- Low-power dissipation Operating: 15 mW/MHz (typical)
- Single power supply voltage of 2.7 to 5.5 V
- Power down features using \overline{CE} .
- Data retention supply voltage of 2.0 to 5.5 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of -40° to 85°C
- Standby Current (maximum):20 µA

• Access Times (maximum):

	TC55NEM208AFPV/AFTV			
	55	70		
Access Time	55 ns	70 ns		
CE Access Time	55 ns	70 ns		
OE Access Time	30 ns	35 ns		

Package:

SOP32-P-525-1.27 (AFPV) (Weight: g typ) TSOP II32-P-400-1.27 (AFTV) (Weight: g typ)

PIN ASSIGNMENT (TOP VIEW)

32 PIN SOP & TSOP

A18 🛛 1	\bigcirc	32 VDD
A16 🛛 2		31 🛛 A15
A14 🛛 3		30 🛛 A17
A12 🛛 4		29 🛛 R/W
A7 🛛 5		28 🛛 A13
A6 🛛 6		27 🛛 A8
A5 🛛 7		26 🛛 A9
A4 🛛 8		25 🛛 A11
A3 🛛 9		24 🛛 🖸
A2 🛛 10	0	23 🛛 A10
A1 🛛 1'	1	22 🛛 CE
A0 🛛 12	2	21 🛛 I/O8
I/O1 □1:	3	20 1/07
I/O2 1/	4	19 🛛 I/O6
I/O3 🛛 1	5	18 🛛 I/O5
GND 1	6	17 🛛 I/O4

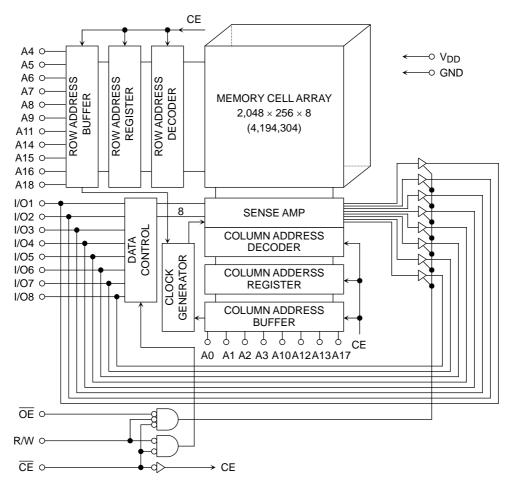
(AFPV/AFTV)

PIN NAMES

A0~A18	Address Inputs
R/W	Read/Write Control
ŌĒ	Output Enable
CE	Chip Enable
I/O1~I/O8	Data Inputs/Outputs
V _{DD}	Power
GND	Ground

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BLOCK DIAGRAM



OPERATING MODE

MODE	CE	ŌĒ	R/W	I/O1~I/O8	POWER
Read	L	L	Н	Output	I _{DDO}
Write	L	*	L	Input	I _{DDO}
Output Deselect	L	н	Н	High-Z	I _{DDO}
Standby	Н	*	*	High-Z	I _{DDS}

* = don't care

H = logic high

L = logic low

MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V _{DD}	Power Supply Voltage	-0.3~7.0	V
V _{IN}	Input Voltage	-0.3*~7.0	V
V _{I/O}	Input/Output Voltage	-0.5~V _{DD} + 0.5	V
PD	Power Dissipation	0.6	W
T _{solder}	Soldering Temperature (10s)	260	°C
T _{stg}	Storage Temperature	-55~150	°C
T _{opr}	Operating Temperature	-40~85	°C

*: -2.0 V when measured at a pulse width of 20ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = -40° to 85° C)

SYMBOL	PARAMETER	$5~V\pm10\%$			UNIT			
STIVIDUL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	2.7	5.0	5.5	V
VIH	Input High Voltage	2.2		$V_{DD} + 0.3$	$V_{DD}-0.2$	_	$V_{DD} + 0.3$	V
VIL	Input Low Voltage	-0.3*		0.6	-0.3*		0.2	V
V _{DH}	Data Retention Supply Voltage	2.0	_	5.5	2.0	_	5.5	V

*: -2.0V when measured at a pulse width of 20 ns

<u>DC CHARACTERISTICS</u> (Ta = -40° to 85°C, V_{DD} = 5 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	TEST CONDITION			TYP	MAX	UNIT
IIL	Input Leakage Current	$V_{IN} = 0 V \sim V_{DD}$			_		±1.0	μA
IOH	Output High Current	V _{OH} = 2.4 V			-1.0	_		mA
I _{OL}	Output Low Current	$V_{OL} = 0.4 V$			2.1	_	_	mA
ILO	Output Leakage Current	$\overline{CE} = V_{IH} \text{ or } R/W = V_{IL} \text{ or } \overline{OE} = V_{IH}, V$	$\overline{CE} = V_{IH} \text{ or } R/W = V_{IL} \text{ or } \overline{OE} = V_{IH}, V_{OUT} = 0 V \sim V_{DD}$				±1.0	μΑ
		$\overline{CE} = V_{IL}$ and R/W = V _{IH} ,		MIN			35	_
IDDO1		I _{OUT} = 0 mA, Other Input = V _{IH} /V _{IL}		1 μs		8		mA
	 Operating Current 	$\overline{CE} = 0.2 \text{ V} \text{ and } \text{R/W} = \text{V}_{\text{DD}} - 0.2 \text{ V},$	MIN	_		30		
IDDO2		I _{OUT} = 0 mA, Other Input = V _{DD} – 0.2 V/0.2 V		1 μs	_	3		mA
I _{DDS1}		CE = V _{IH}	•	•			3	mA
		Та		°C		1		
I _{DDS2}	Standby Current	$\overline{CE} = V_{DD} - 0.2 V,$ $V_{DD} = 2.0 V \sim 5.5 V$	Ta = -40~40°C				3	μA
	V _{DD} = 2.0 V~5.5 V		Ta = -4	0~85°C	_		20	

<u>DC CHARACTERISTICS</u> (Ta = -40° to 85°C, V_{DD} = 3 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	TEST CONDITION			TYP	MAX	UNIT
IIL	Input Leakage Current	$V_{IN} = 0 V \sim V_{DD}$			_		±1.0	μA
I _{OH}	Output High Current	$V_{OH} = V_{DD} - 0.2 V$			-0.1		_	mA
I _{OL}	Output Low Current	V _{OL} = 0.2 V			0.1		_	mA
ILO	Output Leakage Current	$\overline{CE} = V_{IH} \text{ or } R/W = V_{IL} \text{ or } \overline{OE} = V_{IH}, V_{OUT} = 0 V V_{DD}$		_		±1.0	μA	
	Operating Current	$\overline{CE} = 0.2 \text{ V} \text{ and } \text{R/W} = \text{V}_{\text{DD}} - 0.2 \text{ V},$		MIN	_		30	
IDDO2	Operating Current	I _{OUT} = 0 mA, Other Input = V _{DD} – 0.2 V/0.2 V	t _{cycle}	1 μs	_	3	_	mA
			Ta = 25	°C	_	1		
I _{DDS2}	Standby Current	$\overline{CE} = V_{DD} - 0.2 V$	Ta = -40~40°C			—	3	μA
			Ta = -4	0~85°C		_	20	

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C _{IN}	Input Capacitance	$V_{IN} = GND$	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

<u>AC CHARACTERISTICS AND OPERATING CONDITIONS</u> (Ta = -40° to 85°C, V_{DD} = 5 V ± 10%)

READ CYCLE

		TC				
SYMBOL	PARAMETER	5	5	7	0	UNIT
		MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	55	_	70		
tACC	Address Access Time		55	_	70	
t _{CO}	Chip Enable Access Time		55	_	70	
t _{OE}	Output Enable Access Time	_	30	—	35	
t _{COE}	Chip Enable Low to Output Active	5	_	5		ns
tOEE	Output Enable Low to Output Active	0	_	0		
t _{OD}	Chip Enable High to Output High-Z		25	_	30	
todo	Output Enable High to Output High-Z		25	_	30	
t _{OH}	Output Data Hold Time	10	—	10	_	

WRITE CYCLE

		TC				
SYMBOL	PARAMETER	5	5	7	0	UNIT
		MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	55	_	70		
t _{WP}	Write Pulse Width	40	_	50	_	
t _{CW}	Chip Enable to End of Write	45	_	55	_	
t _{AS}	Address Setup Time	0	_	0		
t _{WR}	Write Recovery Time	0	_	0		ns
t _{ODW}	R/W Low to Output High-Z	_	25	_	30	
t _{OEW}	R/W High to Output Active	0	_	0		
t _{DS}	Data Setup Time	25	_	30		
t _{DH}	Data Hold Time	0	_	0		

AC TEST CONDITIONS

PARAMETER	TEST CONDITION
Output load	100 pF + 1 TTL Gate
Input pulse level	0.4 V, 2.4 V
Timing measurements	1.5 V
Reference level	1.5 V
t _R , t _F	5 ns

AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = -40° to 85°C, V_{DD}=2.7 to 5.5 V)

READ CYCLE

SYMBOL	PARAMETER	TC55NEM208AFPV/AFTV				
		55		70		UNIT
		MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	70	_	85	_	
tACC	Address Access Time	_	70		85	
t _{CO}	Chip Enable Access Time	_	70		85	
t _{OE}	Output Enable Access Time	—	35		45	
t _{COE}	Chip Enable Low to Output Active	5	_	5	_	ns
tOEE	Output Enable Low to Output Active	0	_	0	_	
t _{OD}	Chip Enable High to Output High-Z	_	30		35	
todo	Output Enable High to Output High-Z	_	30		35	
t _{OH}	Output Data Hold Time	10	_	10	_	

WRITE CYCLE

SYMBOL	PARAMETER	TC55NEM208AFPV/AFTV				
		55		70		UNIT
		MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	70	_	85		
t _{WP}	Write Pulse Width	50	_	55		
t _{CW}	Chip Enable to End of Write	55	_	60	_	
t _{AS}	Address Setup Time	0	_	0		
t _{WR}	Write Recovery Time	0	_	0		ns
t _{ODW}	R/W Low to Output High-Z	_	30	_	35	
t _{OEW}	R/W High to Output Active	0	_	0		
t _{DS}	Data Setup Time	30	_	35		
t _{DH}	Data Hold Time	0	_	0		

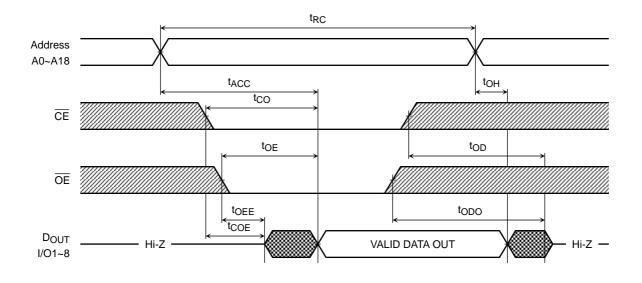
AC TEST CONDITIONS

PARAMETER	TEST CONDITION		
Output load	100 pF (Include Jig)		
Input pulse level	0.2 V, V _{DD} – 0.2 V		
Timing measurements	1.5 V		
Reference level	1.5 V		
t _R , t _F	5 ns		

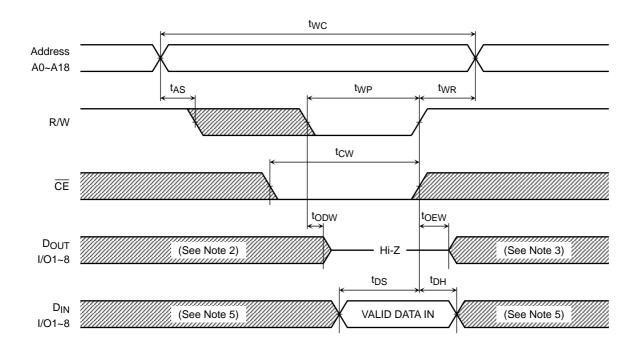
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TIMING DIAGRAMS

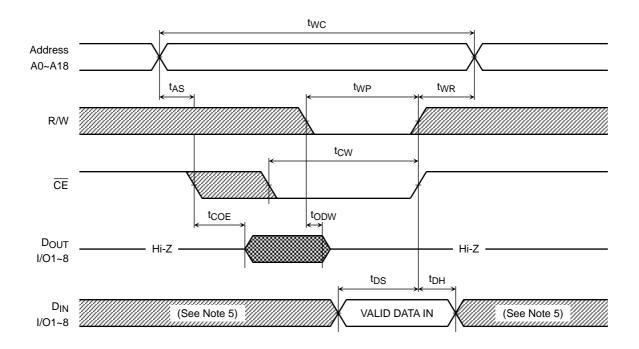
READ CYCLE (See Note 1)



WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



WRITE CYCLE 2 (CE CONTROLLED) (See Note 4)



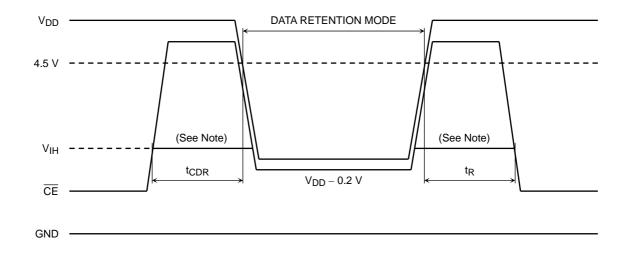
Note:

- (1) R/W remains HIGH for the read cycle.
- (2) If \overline{CE} goes LOW coincident with or after R/W goes LOW, the outputs will remain at high impedance.
- (3) If \overline{CE} goes HIGH coincident with or before R/W goes HIGH, the outputs will remain at high impedance.
- (4) If \overline{OE} is HIGH during the write cycle, the outputs will remain at high impedance.
- (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = -40° to 85°C)

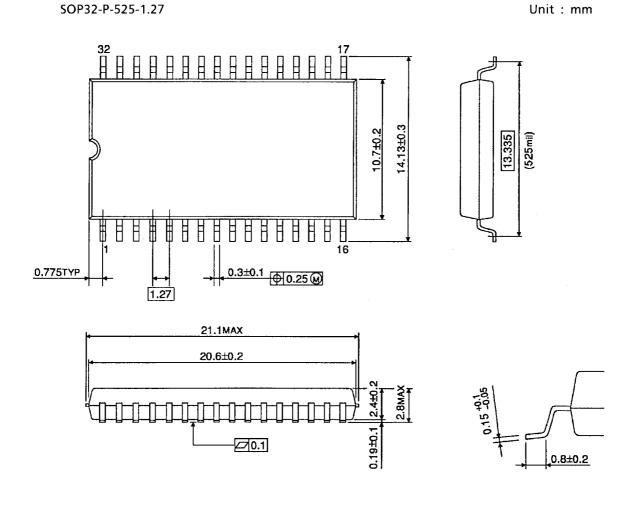
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V _{DH}	Data Retention Supply Voltage		2.0	_	5.5	V
IDDS2	Standby Current	Ta = -40~40°C		_	3	۵
		Ta = -40~85°C	_	_	20	μΑ
t _{CDR}	Chip Deselect to Data Retention Mode Time		0	_	_	ns
t _R	Recovery Time	5	_	_	ms	

CE CONTROLLED DATA RETENTION MODE



Note: When \overline{CE} is operating at the V_{IH} level (2.2V), the standby current is given by I_{DDS1} during the transition of V_{DD} from 4.5 to 2.4V.

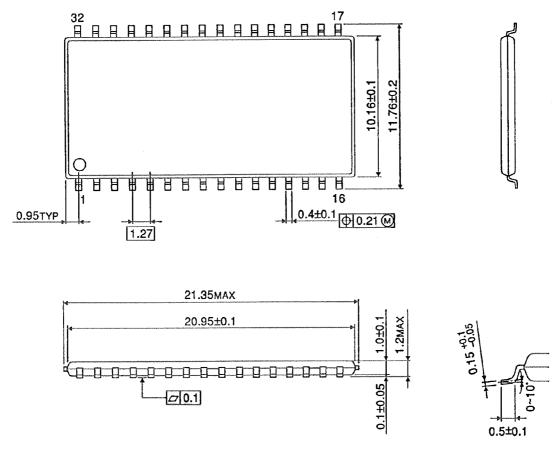
PACKAGE DIMENSIONS



Weight: g (typ)

PACKAGE DIMENSIONS

Unit: mm



Weight: g (typ)

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